CLAIMS

What is claimed is:

1. A memory circuit, comprising:

a memory array comprising a plurality of memory cells; and

a memory control circuit operable to generate one or more control signals for performing memory operations on memory cells within the memory array, the memory control circuit including a cycle ready circuit operable to generate a control signal for initiation of a second memory operation a predetermined period of time after detection of completion of a first memory operation, wherein the predetermined period of time corresponds to an amount of time needed for a true and complement bit line associated with a memory cell associated with the second memory operation to substantially equalize and reach a predetermined voltage level.

2. The memory circuit of claim 1, wherein the cycle ready circuit comprises a row load circuit having a loading that corresponds to a number of rows in the memory array, wherein a signal propagating therethrough is delayed an amount corresponding to a time needed for the true and complement bit lines to reach the predetermined level.

3. The memory circuit of claim 2, wherein the row load circuit comprises a dummy bit line having a length corresponding to the true and complement bit lines in the memory array.

4. The memory circuit of claim 3, wherein the dummy bit line further comprises a plurality of dummy bit cell transistors coupled thereto, wherein the plurality of dummy bit cell transistors correspond to a number of bit cell transistors coupled to the true and complement bit lines, respectively.

5. The memory circuit of claim 2, wherein the row load circuit further comprises a tuning element operable to vary the loading and thus the signal delay of the row load circuit.

6. The memory circuit of claim 5, wherein the tuning element comprises one or more programmable fuses associated with a dummy bit line, wherein an opening or closing of the one or more programmable fuses alters the loading associated with the dummy bit line.

7. The memory circuit of claim 1, wherein the cycle ready circuit comprises a diode loading circuit having a loading associated therewith that increases as a power supply voltage associated with the memory circuit decreases, thereby increasing the predetermined period of time as the power supply voltage decreases.

8. The memory circuit of claim 7, wherein the diode loading circuit comprises:

a first inverter having an input and an output;

a second inverter having an input coupled to the output of the first inverter, and an output; and

a diode selectively coupled to the input of the second inverter based on a state of the output of the second inverter, wherein when the output of the second inverter is high, the diode is coupled to the input of the second inverter, pulling the input low, and wherein when the output of the first inverter goes low, the diode is slowly decoupled from the input of the second inverter, thereby defining a rate by which the output of the second inverter transitions from high to low.

9. The memory circuit of claim 9, wherein a rate in which the diode is decoupled from the input of the second inverter decreases when the supply voltage decreases, thereby slowing the rate by which the output of the second inverter transitions from high to low when the supply voltage decreases.

10. The memory circuit of claim 1, wherein an input signal into the cycle ready circuit comprises a bit line precharge enable signal.

11. The memory circuit of claim 1, wherein the cycle ready circuit further comprises a pulse generator in series with a delay circuit, wherein the delay circuit delays a signal transmission therethrough by a time period associated with the predetermined period of time needed for the true and complement bit lines to substantially equalize and reach the predetermined voltage level.

12. The memory circuit of claim 11, wherein the pulse generator comprises:

a logic circuit having a first input, a second input, and an output; and

a delay chain coupled to the second input of the logic circuit, wherein an input signal is coupled to the first input and the delay chain, and wherein the logic circuit outputs a pulse having a pulse width related to a signal propagation delay through the delay chain.

13. In combination with a memory array comprising a plurality of memory cells, a memory control circuit operable to generate one or more control signals for initiation of memory operations associated with the memory array, the control circuit comprising a cycle ready circuit operable to generate a cycle ready strobe signal for initiating a next memory operation after an initial memory operation based on identification of a completion of the initial memory operation.

14. The memory control circuit of claim 13, wherein the cycle ready circuit is operable to generate the cycle ready strobe signal to initiate the next memory operation a predetermined period of time after completion of the initial memory operation is identified, wherein the predetermined period of time is sufficient to ensure that a true and complement bit line associated with a selected memory cell in the memory array have substantially equalized and reached a predetermined value.

15. The memory control circuit of claim 14, wherein the predetermined period of time varies with respect to a number of rows in the memory array, a supply voltage, or both.

16. The memory control circuit of claim 14, wherein the cycle ready circuit comprises a row load circuit operable to propagate a control signal therethrough, wherein a propagation delay of the control signal through the row load circuit corresponds to a number of rows in the memory array.

17. The memory control circuit of claim 16, wherein the row load circuit comprises a dummy bit line having a length corresponding to the true and complement bit lines associated with the selected memory cell in the memory array.

18. The memory circuit of claim 17, wherein the dummy bit line further comprises a plurality of dummy bit cell transistors coupled thereto, wherein the plurality of dummy bit cell transistors correspond to a number of bit cell transistors coupled to the true and complement bit lines, respectively.

19. The memory circuit of claim 17, wherein the row load circuit further comprises a tuning element operable to vary the loading and thus the signal propagation delay of the row load circuit.

20. The memory circuit of claim 19, wherein the tuning element comprises one or more programmable fuses associated with a dummy bit line, wherein an opening or closing of the one or more programmable fuses alters the loading associated with the dummy bit line.

21. The memory control circuit of claim 14, wherein the cycle ready circuit comprises a diode loading circuit operable to propagate a control signal therethrough, wherein a propagation delay of the control signal through the diode loading circuit corresponds to a supply voltage associated with the memory array.

22. The memory circuit of claim 21, wherein the propagation delay associated with the diode loading circuit increases as a power supply voltage associated with the memory array decreases, thereby increasing the predetermined period of time as the power supply voltage decreases.

23. The memory circuit of claim 22, wherein the diode loading circuit comprises:

a first inverter having an input and an output;

a second inverter having an input coupled to the output of the first inverter, and an output; and

a diode selectively coupled to the input of the second inverter based on a state of the output of the second inverter, wherein when the output of the second inverter is high, the diode is coupled to the input of the second inverter, pulling the input low, and wherein when the output of the first inverter goes low, the

diode is slowly decoupled from the input of the second inverter, thereby defining a rate by which the output of the second inverter transitions from high to low.

24. The memory circuit of claim 23, wherein a rate in which the diode is decoupled from the input of the second inverter decreases when the supply voltage decreases, thereby slowing the rate by which the output of the second inverter transitions from high to low when the supply voltage decreases.

25. The memory circuit of claim 14, wherein a control signal into the cycle ready circuit associated with completion of the initial memory operation comprises a bit line precharge enable signal.

26. The memory circuit of claim 14, wherein the cycle ready circuit further comprises a pulse generator in series with a delay circuit, wherein the delay circuit delays a signal transmission therethrough by a time period associated with the predetermined period of time needed for the true and complement bit lines to substantially equalize and reach the predetermined voltage level.

27. The memory circuit of claim 26, wherein the pulse generator comprises:

a logic circuit having a first input, a second input, and an output; and

a delay chain coupled to the second input of the logic circuit, wherein an input signal is coupled to the first input and the delay chain, and wherein the logic circuit outputs a pulse having a pulse width related to a signal propagation delay through the delay chain.